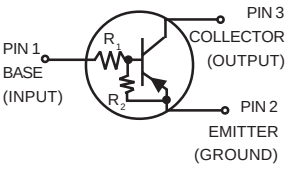
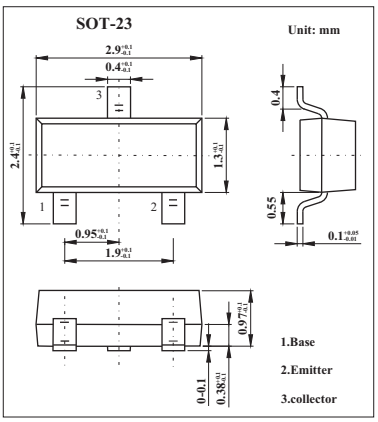
PNP Silicon Bias Resistor Transistor

KMUN2114

■ Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count





■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Collector-base voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	50	V
Collector Current -Continuous	I_C	0.1	A
Collector Power dissipation	P_C	0.24	W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	508	℃/W
Junction temperature	T_j	150	℃
Storage temperature	T_{stg}	-55 to +150	℃

■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Collector-base breakdown voltage	$V_{(BR)CBO}$	I_C= 10 μA, I_E=0	50			V
Collector-emitter breakdown voltage	$V_{(BR)CEO}$	I_C= 2mA, I_B=0	50			V
Collector cut-off current	I_{CBO}	V_{CB}= 50 V , I_E=0			0.1	μA
Collector cut-off current	I_{CEO}	V_{CE}= 50 V , I_B=0			0.5	μA
Emitter cut-off current	I_{EBO}	V_{EB}= 6V , I_C=0			0.2	mA
DC current gain	h_{FE}	V_{CE}=10V, I_C= 5.0mA	80	140		
Collector-emitter saturation voltage	$V_{CE(sat)}$	I_C = 10 mA, I_B = 0.3 mA			0.25	V
Output Voltage (on)	V_{OL}	V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0kΩ			0.2	V
Output Voltage (off)	V_{OH}	V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ	4.9			V
Input Resistor	R_1		7 .0	10	13	kΩ
Resistor Ratio	R_1/R_2		0.17	0.21	0.25	

■ Marking

Marking	A6D

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■ Typical Characteristics

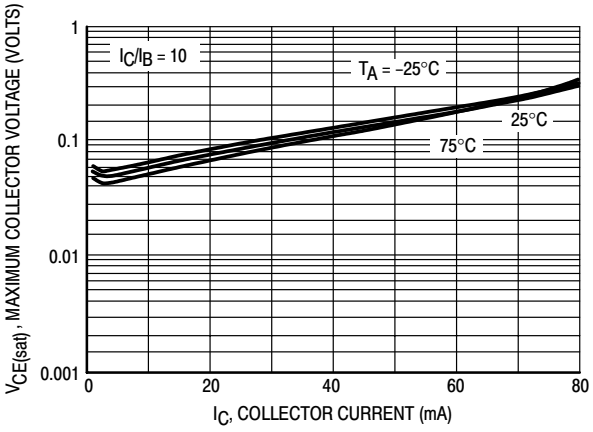

Figure 17. $V_{CE(sat)}$ versus I_C

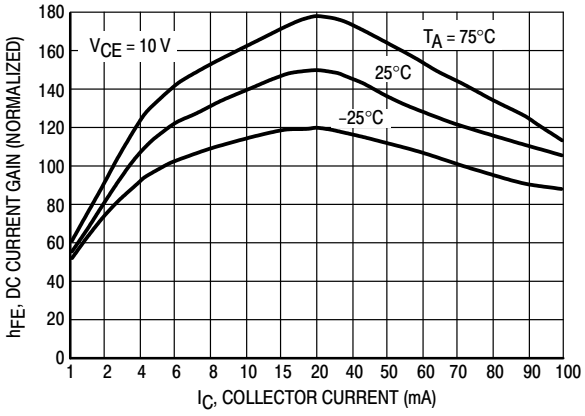

Figure 18. DC Current Gain

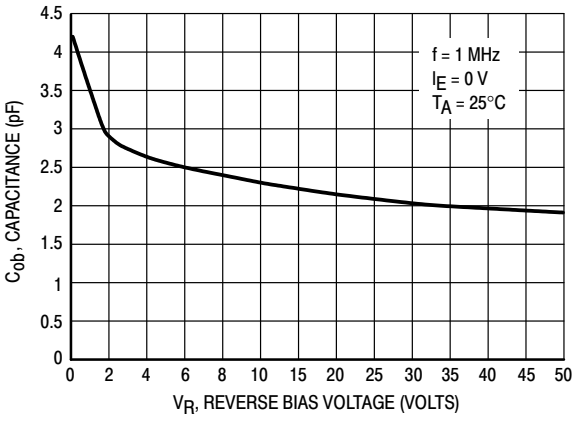

Figure 19. Output Capacitance

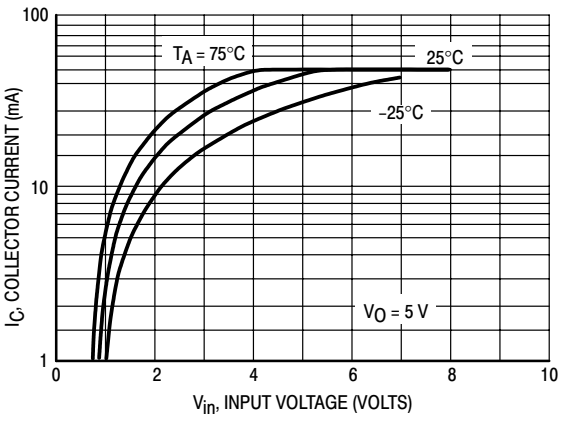

Figure 20. Output Current versus Input Voltage

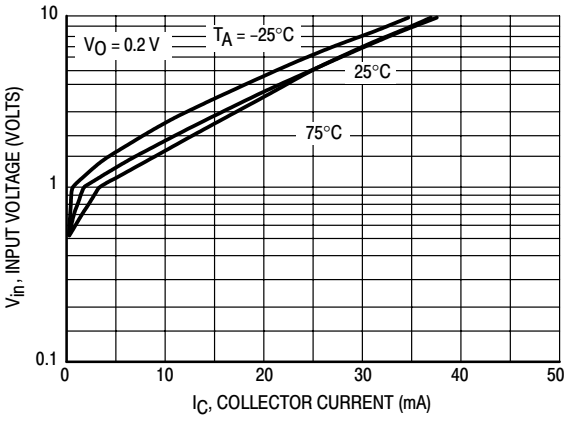

Figure 21. Input Voltage versus Output Current

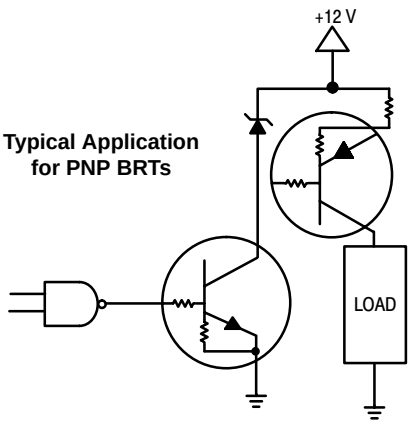

Figure 22. Inexpensive, Unregulated Current Source