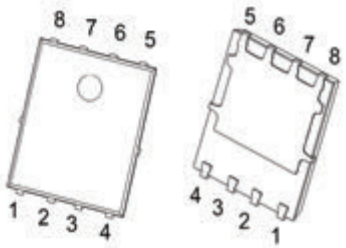
N-Channel MOSFET

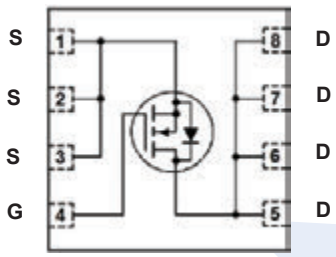
2KK5081DFN

■ Features

- V_{DS} = 100 V
- I_D (at V_{GS}=10V) = 100 A
- $R_{DS(ON)}$ (at V_{GS} = 10 V) < 4.2 mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5 V) < 6.0 mΩ
- 100% UIS Tested
- 100% R_g Tested

PDFN5x6-8(PDFNWB5x6-8L)





■ Absolute Maximum Ratings (T_A = 25℃ unless otherwise noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25℃	I_D	100	A
	T_C = 100℃		100	
Pulsed Drain Current (Note 2)		I_{DM}	320	
Continuous Drain Current	T_A = 25℃	I_{DSM}	30.5	
	T_A = 70℃		24.5	
Avalanche Current (Note 2)		I_{AS}	65	A
Avalanche Energy L = 0.1mH (Note 2)		E_{AS}	211	mJ
Thermal Resistance, Junction- to-Ambient (Note 5)		$R_{\theta JA}$	50	℃/W
Thermal Resistance, Junction- to-Case		$R_{\theta JC}$	0.58	
Power Dissipation (Note 4)	T_C = 25℃	P_D	215	W
	T_C = 100℃		86	
Power Dissipation (Note 5)	T_A = 25℃	P_{DSM}	6.2	
	T_A = 70℃		4.0	
Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{stg}	-55 to 150	

Notes:

1. The maximum current rating is package limited.
2. Single pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
3. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
4. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
5. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

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■ Electrical Characteristics (T_J = 25℃ unless othewise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250 μA, V_{GS} = 0V	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			1	μA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J=55℃			5	
Gate to Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 250μA	2.3		4.3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 20 A		3.7	4.2	mΩ
		V_{GS} = 10 V, I_D = 20 A, T_J=125℃			6.8	
		V_{GS} = 4.5 V, I_D = 20 A			6.0	
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 20 A		100		S
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz		5940		pF
Output Capacitance	C_{oss}			1475		
Reverse Transfer Capacitance	C_{rss}			24		
Gate Resistance	R_g	V_{GS}=0V, V_{DS}=0V, f = 1MHz	0.3	0.6	1.0	Ω
Switching Characteristics						
Total Gate Charge (10V)	Q_g	V_{GS} = 10V, V_{DS} = 50 V, I_D = 20 A		80	115	nC
Total Gate Charge (4.5V)				35	50	
Gate Source Charge	Q_{gs}			18		
Gate Drain Charge	Q_{gd}			11		
Turn-On DelayTime	$t_{d(on)}$	V_{GS} = 10V, V_{DS} = 50 V, R_L = 2.5 Ω, R_{GEN} = 3 Ω		16.5		ns
Turn-On Rise Time	t_r			6.5		
Turn-Off DelayTime	$t_{d(off)}$			46		
Turn-Off Fall Time	t_f			12		
Drain-Source Diode Characteristics						
Body Diode Reverse Recovery Time	t_{rr}	I_F = 20A, dI/dt = 500 A/μs		43		ns
Body Diode Reverse Recovery Charge	Q_{rr}			207		nC
Maximum Body-Diode Continuous Current	I_S	(Note 1)			100	A
Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1 A		0.68	1	V

Notes:

6. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
7. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.
8. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

■ Marking

Marking	K5081 KC***

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■ Typical Electrical and Thermal Characteristics

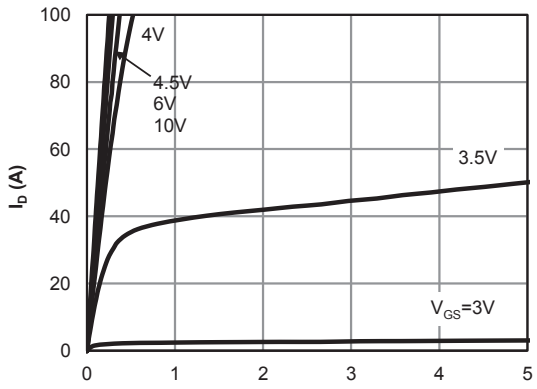

Figure 1: On-Region Characteristics (NOTE 6)

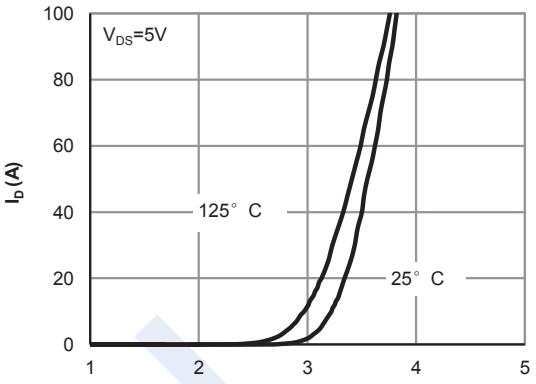

Figure 2: Transfer Characteristics (NOTE 6)

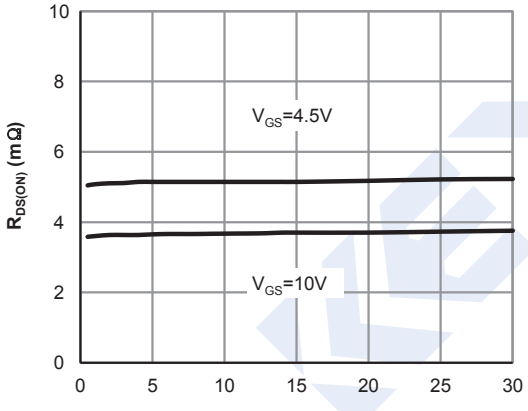

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (NOTE 6)

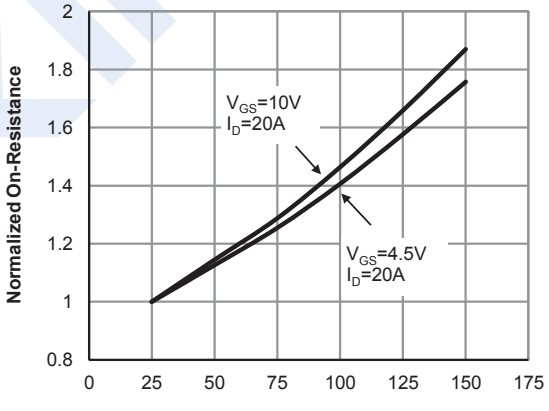

Figure 4: On-Resistance vs. Junction Temperature (NOTE 6)

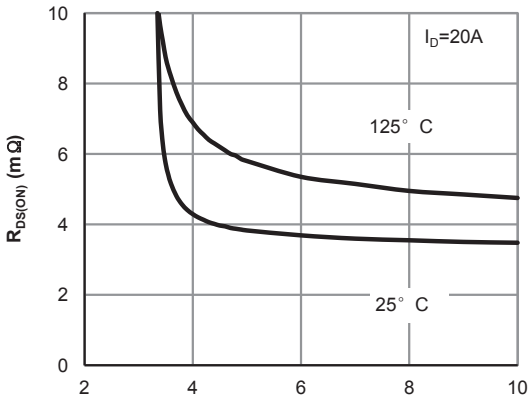

Figure 5: On-Resistance vs. Gate-Source Voltage (NOTE 6)

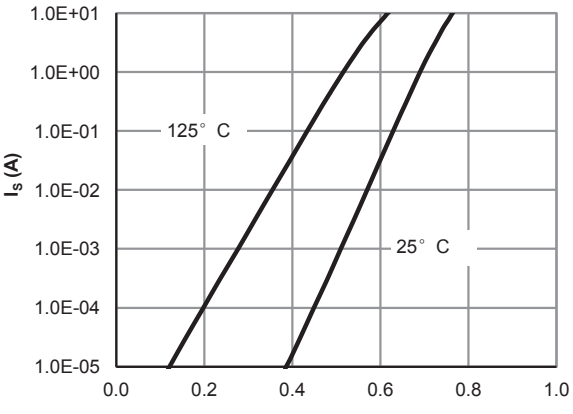

Figure 6: Body-Diode Characteristics (NOTE 6)

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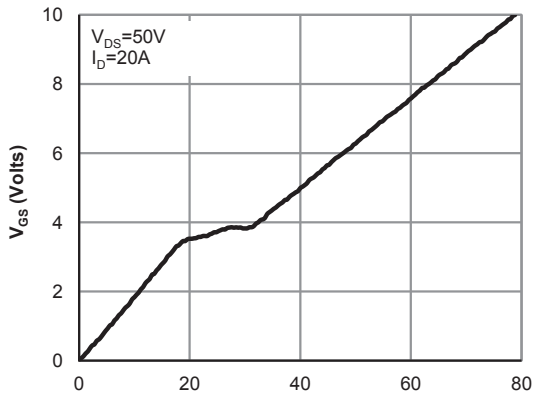

Figure 7: Gate-Charge Characteristics

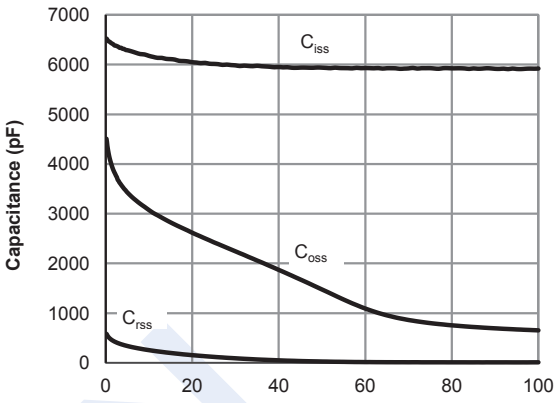

Figure 8: Capacitance Characteristics

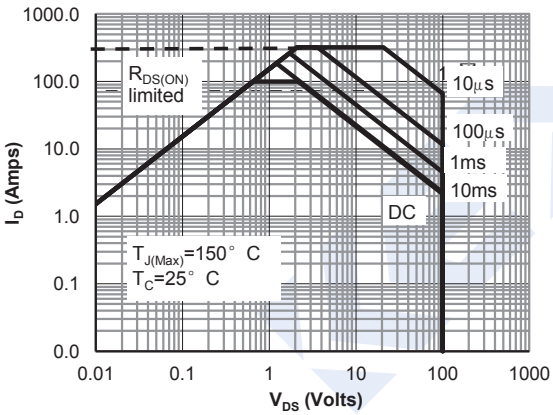

Figure 9: Maximum Forward Biased Safe Operating Area (NOTE 7)

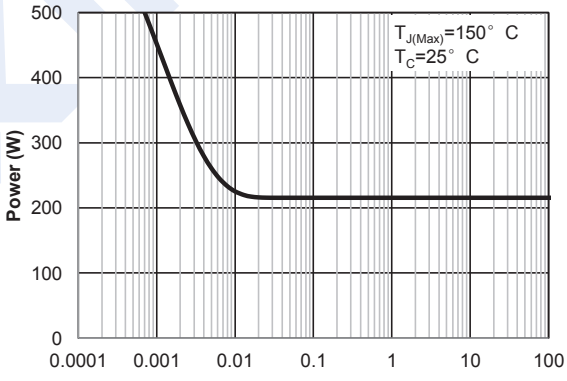

Figure 10: Single Pulse Power Rating Junction-to-Case (NOTE 7)

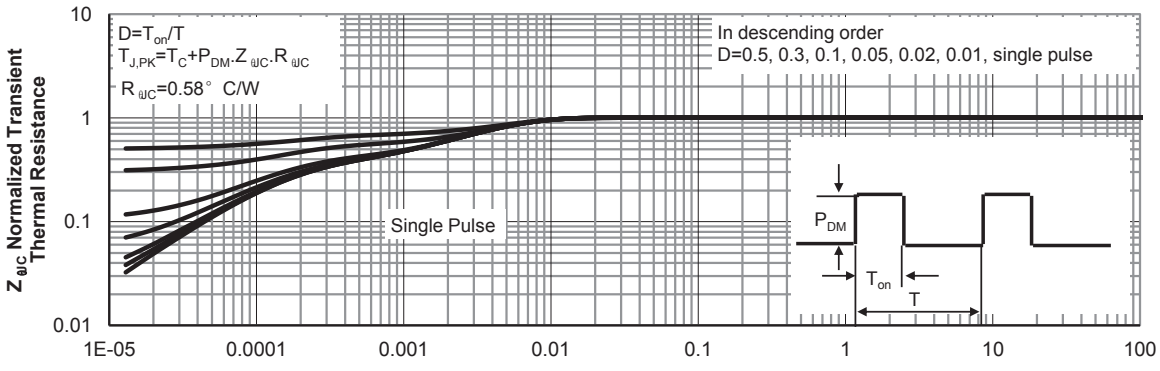

Figure 11: Normalized Maximum Transient Thermal Impedance (NOTE 7)

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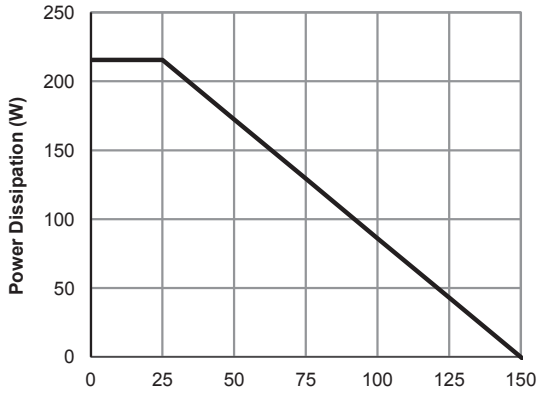

Figure 12: Power De-rating (NOTE 7)

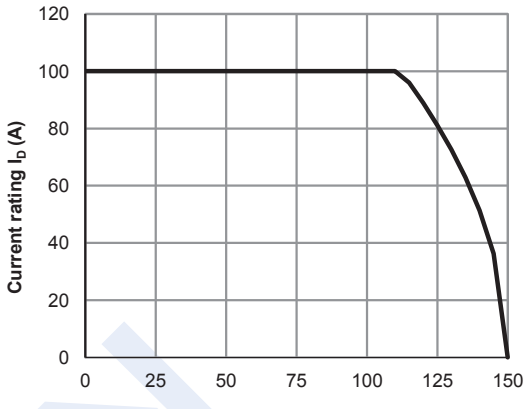

Figure 13: Current De-rating (NOTE 7)

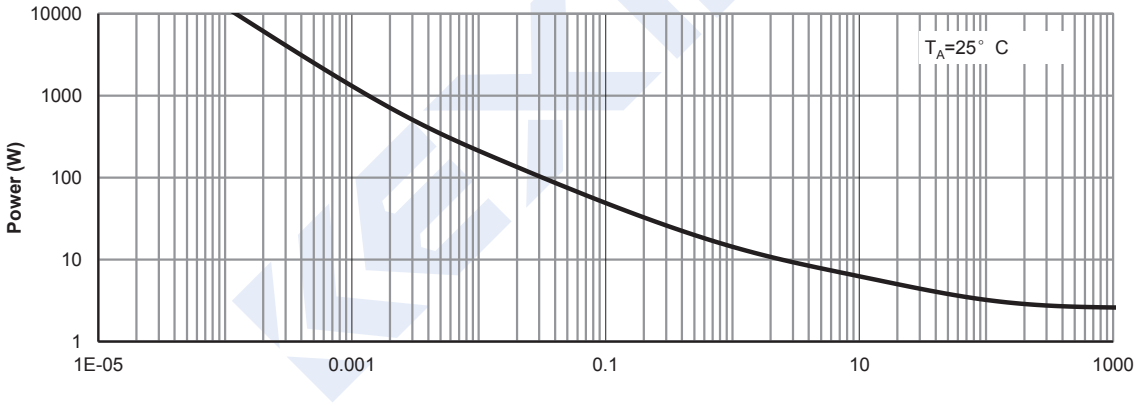

Figure 14: Single Pulse Power Rating Junction-to-Ambient (NOTE 8)

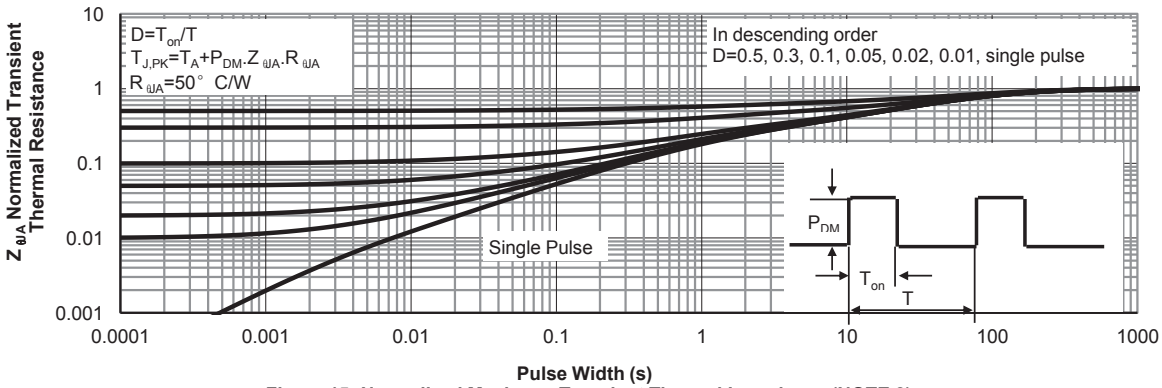

Figure 15: Normalized Maximum Transient Thermal Impedance (NOTE 8)

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Figure A: Gate Charge Test Circuit & Waveforms

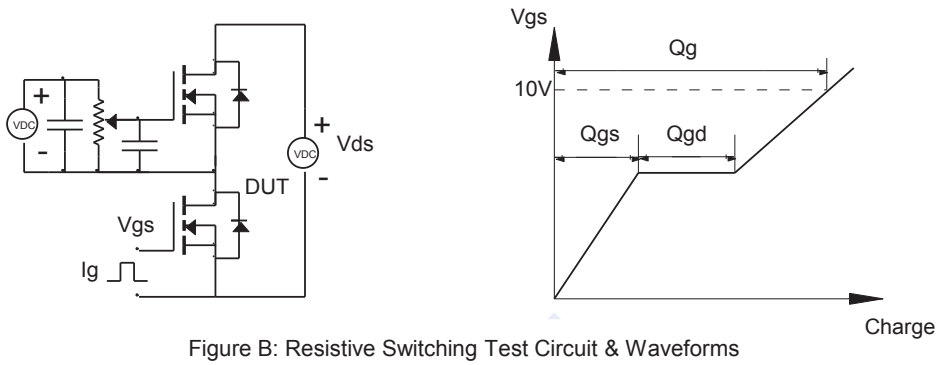


Figure B: Resistive Switching Test Circuit & Waveforms

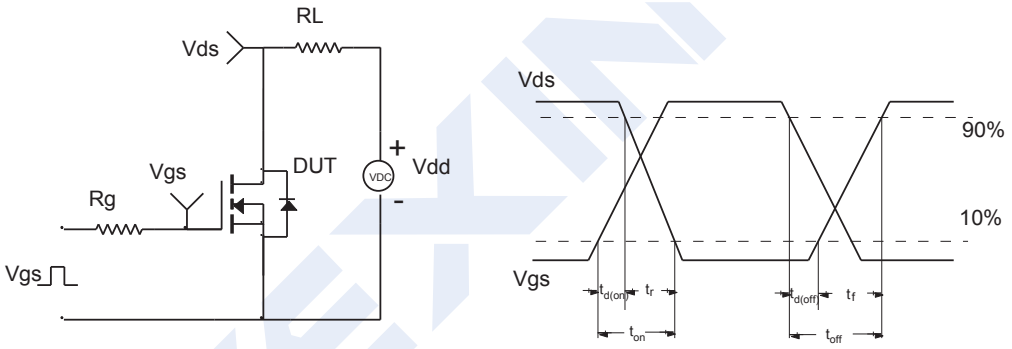


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

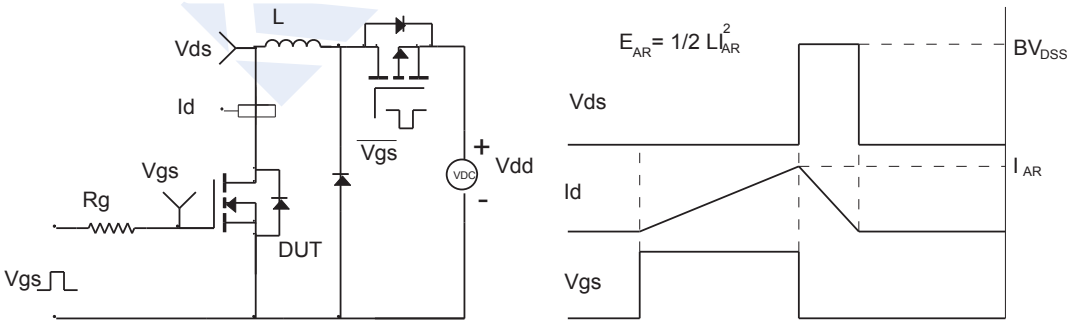
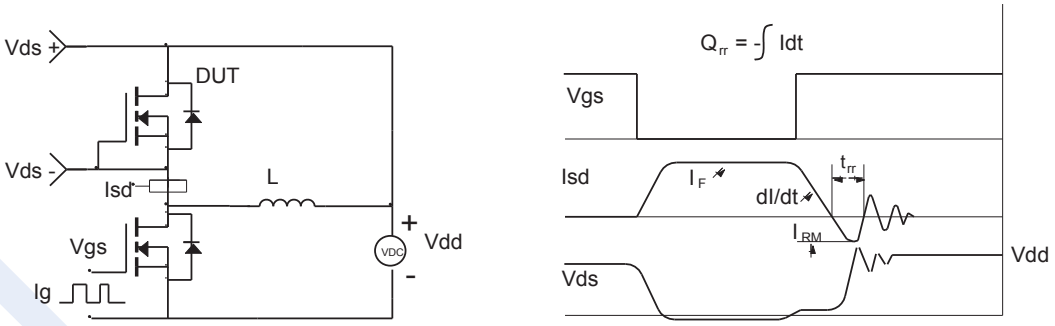


Figure D: Diode Recovery Test Circuit & Waveforms



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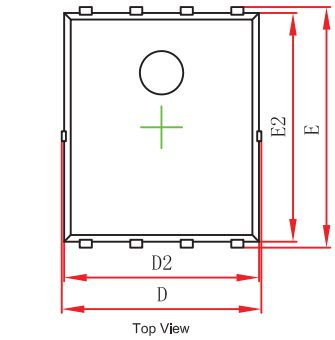
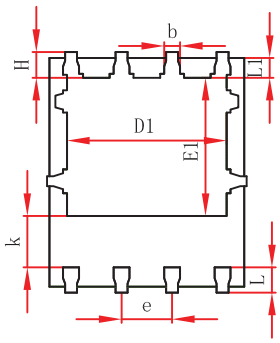
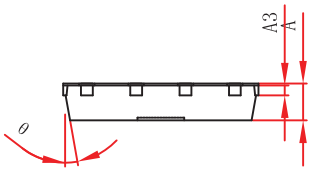
■ PDFN5x6-8(PDFNWB5x6-8L) Package Outline Dimensions



Top View

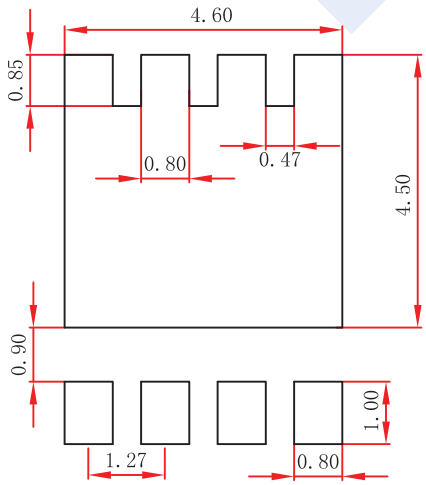


Bottom View



Side View

■ PDFN5x6-8(PDFNWB5x6-8L) Suggested Pad Layout



Note:

1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.