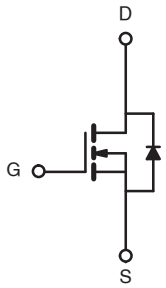
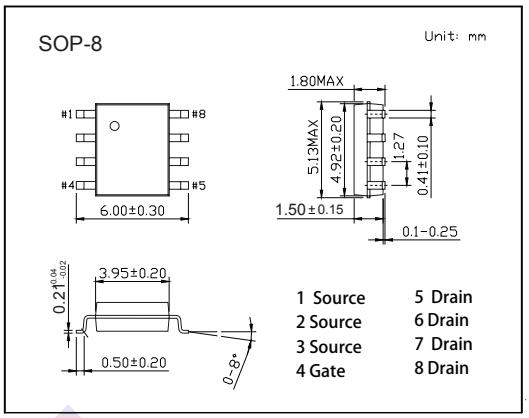
N-Channel MOSFET

2KK7006

■ Features

- V_{DS} = 100 V
- I_D (at V_{GS} = 10 V) = 13.5 A
- $R_{DS(ON)}$ (at V_{GS} = 10 V) < 8.3 mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5 V) < 10.6 mΩ





■ Absolute Maximum Ratings (T_A = 25℃ unless otherwise noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A=25℃	I_D	13.5	A
	T_A=70℃		10.5	
Pulsed Drain Current [C]		I_{DM}	55	
Avalanche Current [C]		I_{AS}	33	
Avalanche Energy L = 0.1 mH [C]		E_{AS}	54	mJ
V_{DS} Spike	10μs	V_{SPIKE}	120	V
Power Dissipation [B]	T_A=25℃	P_D	3.1	W
	T_A=70℃		2.0	
Thermal Resistance, Junction- to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	40	℃/W
Thermal Resistance, Junction- to-Ambient [A D]	Steady-State		75	
Thermal Resistance, Junction- to-Lead	Steady-State	$R_{\theta JL}$	24	
Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{stg}	-55 to 150	

Notes:

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤10s junction-to-case thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in^2 FR-4 board with 2oz Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

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■ Electrical Characteristics (T_J = 25℃ unless othewise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250 μA, V_{GS} = 0V	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			1	μA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 55 ℃			5	
Gate to Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 250μA	1.3		2.3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 13.5 A			8.3	mΩ
		V_{GS} = 10 V, I_D = 13.5 A, T_J = 125 ℃			14.8	
		V_{GS} = 4.5 V, I_D = 11.5 A			10.6	
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 13.5 A		75		S
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz		3130		pF
Output Capacitance	C_{oss}			245		
Reverse Transfer Capacitance	C_{rss}			12.5		
Gate Resistance	R_g	V_{GS} = 0 V, V_{DS} = 0 V, f = 1 MHz	0.7	1.4	2.1	Ω
Total Gate Charge	Q_g(10V)	V_{GS} = 10V, V_{DS} = 50 V, I_D = 13.5 A		42	60	nC
Total Gate Charge	Q_g(4.5V)			18.5	28	
Gate Source Charge	Q_{gs}			7.5		
Gate Drain Charge	Q_{gd}			4.5		
Turn-On DelayTime	$t_{d(on)}$	V_{GS} = 10V, V_{DS} = 50 V, R_L = 3.7 Ω, R_{GEN} = 3 Ω		8		ns
Turn-On Rise Time	t_r			5		
Turn-Off DelayTime	$t_{d(off)}$			41		
Turn-Off Fall Time	t_f			7		
Body Diode Reverse Recovery Time	t_{rr}	I_F = 13.5 A, dI/dt = 500 A/μs		28		
Body Diode Reverse Recovery Charge	Q_{rr}			130		nC
Maximum Body-Diode Continuous Current	I_S				4	A
Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1 A		0.7	1	V

■ Marking

Marking	K7006 KC****

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■ Typical Electrical and Thermal Characteristics

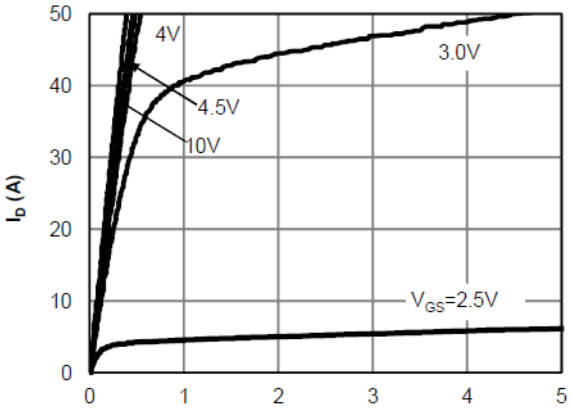

Figure 1: On-Region Characteristics (Note E)

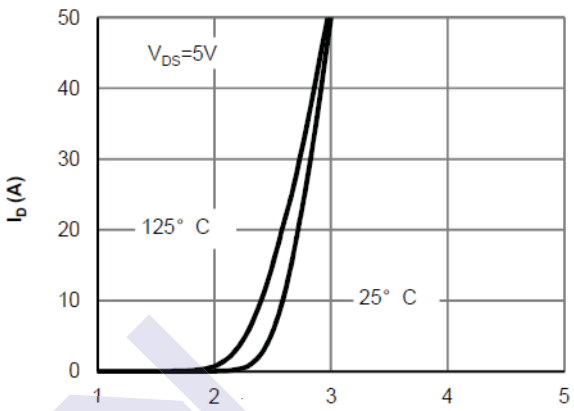

Figure 2: Transfer Characteristics (Note E)

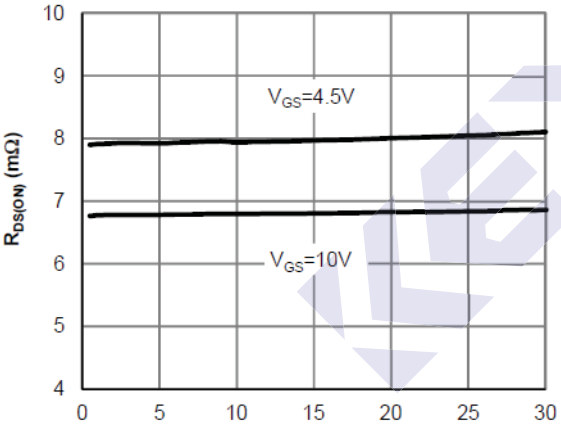

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

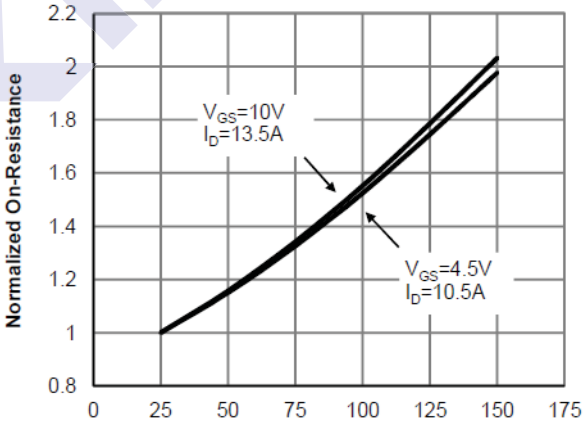

Figure 4: On-Resistance vs. Junction Temperature (Note E)

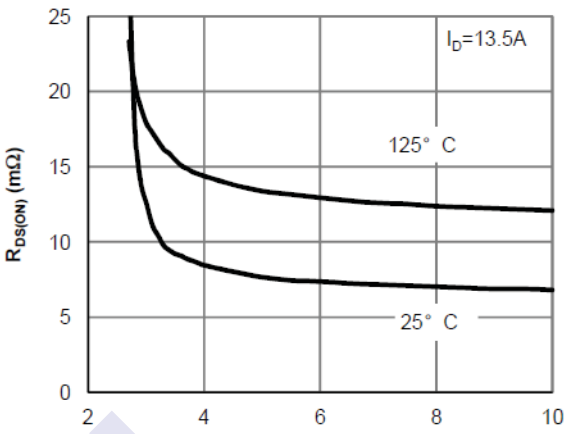

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

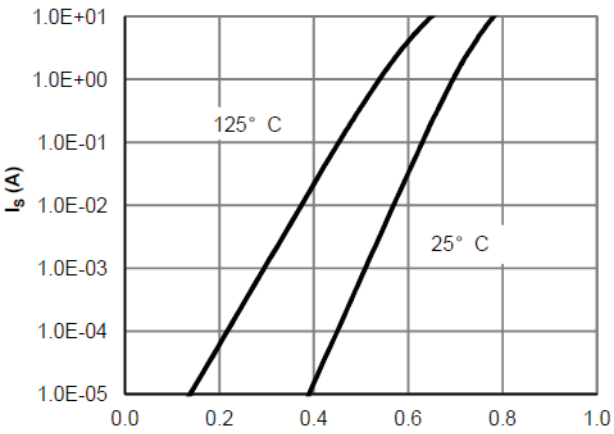

Figure 6: Body-Diode Characteristics (Note E)

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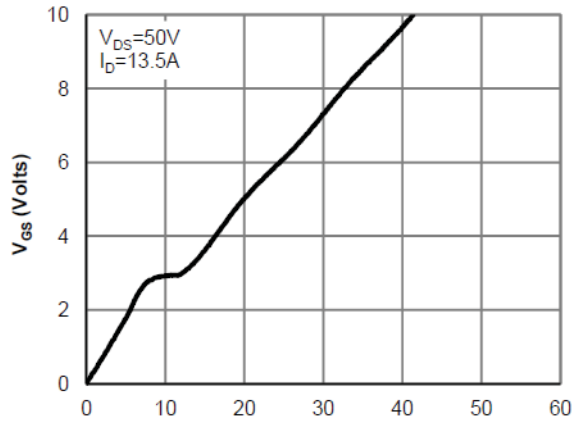

Figure 7: Gate-Charge Characteristics

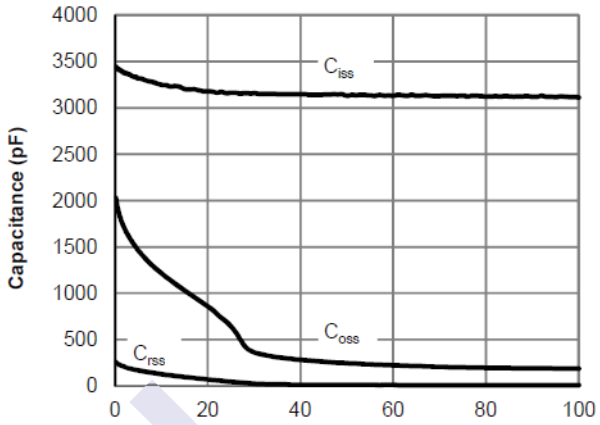

Figure 8: Capacitance Characteristics

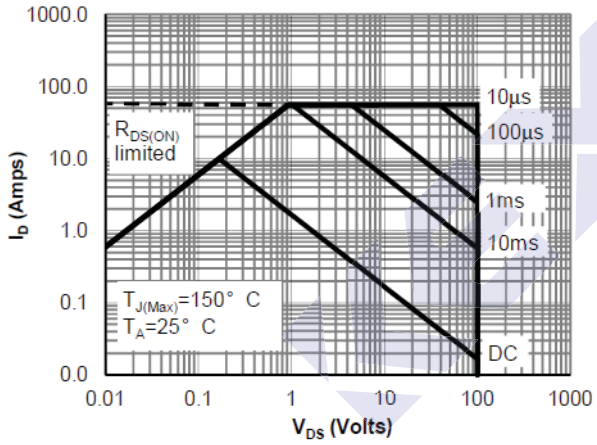

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

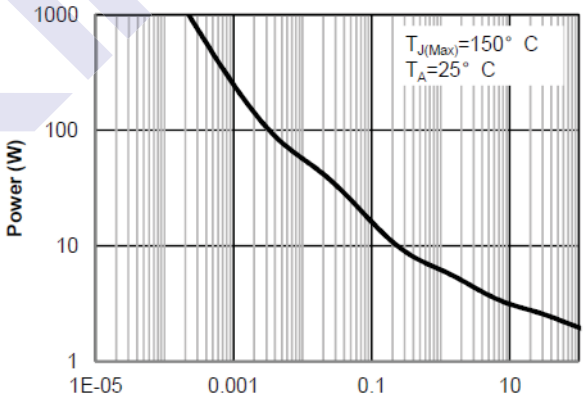

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

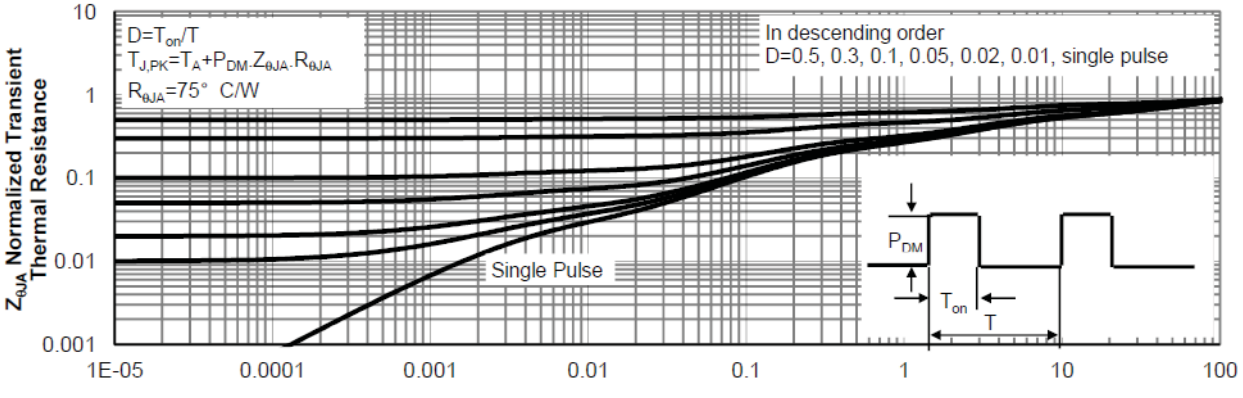

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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Figure A: Gate Charge Test Circuit & Waveforms

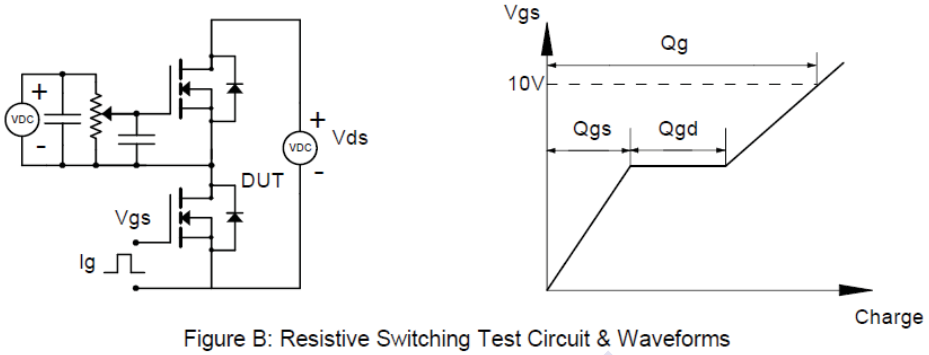

Figure B: Resistive Switching Test Circuit & Waveforms

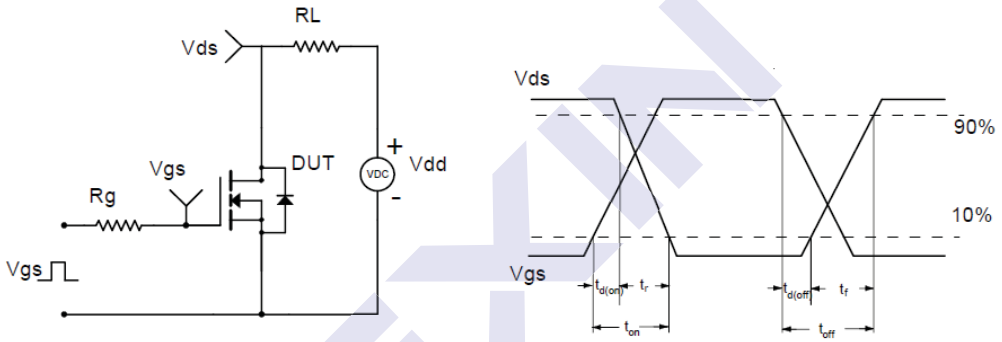

Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

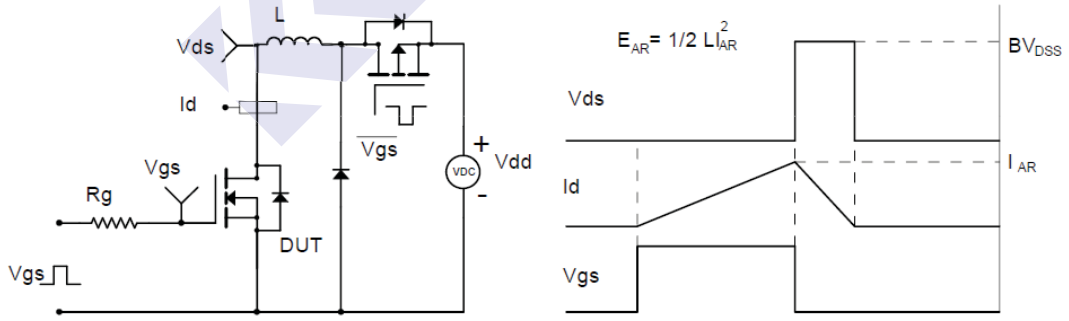

Figure D: Diode Recovery Test Circuit & Waveforms