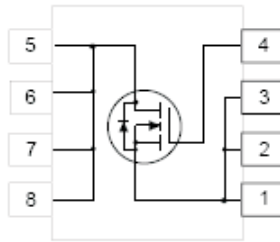
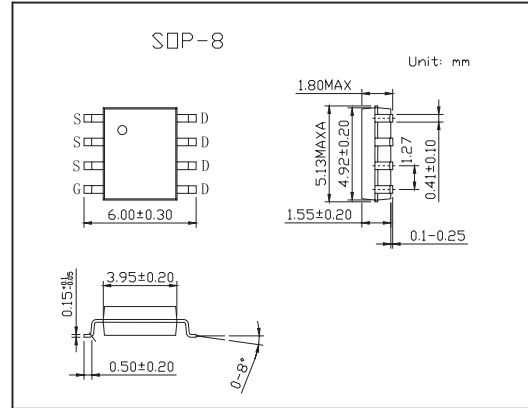


80V N-Channel PowerTrench MOSFET

KDS3512

■ Features

- 4.0 A, 80 V. $R_{DS(ON)} = 70\text{m}\Omega$ @ $V_{GS} = 10\text{ V}$
 $R_{DS(ON)} = 80\text{m}\Omega$ @ $V_{GS} = 6\text{ V}$
- Low gate charge (13 nC typical)
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DS}	80	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current Continuous (Note 1a)	I_D	4	A
Drain Current Pulsed		30	A
Power dissipation (Note 1a)	P_D	2.5	W
Power dissipation (Note 1b)		1.2	
Power dissipation (Note 1c)		1	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	25	$^\circ\text{C/W}$

KDS3512

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Single Pulse Drain-Source Avalanche Energy	WDSS	V _{DD} = 40 V, I _D = 4.0A (Not 2)			90	mJ
Maximum Drain-Source Avalanche Current	I _{AR}	(Not 2)			4.0	A
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 250 μA	80			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I _D = 250 μA, Referenced to 25°C		80		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 64 V, V _{GS} = 0 V			1	μA
Gate-Body Leakage, Forward	I _{GSSF}	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
Gate-Body Leakage, Reverse	I _{GSSR}	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	2.4	4	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I _D = 250 μA, Referenced to 25°C		-6		mV/°C
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 4.0 A		50	70	mΩ
		V _{GS} = 6 V, I _D = 3.7 A		55	80	
		V _{GS} = 10 V, I _D = 4.0 A, T _J = 125°C		91	135	
On-State Drain Current	I _{D(on)}	V _{GS} = 10 V, V _{DS} = 5 V	20			A
Forward Transconductance	g _{FS}	V _{DS} = 10V, I _D = 4.0 A		14		S
Input Capacitance	C _{iss}	V _{DS} = 40 V, V _{GS} = 0 V, f = 1.0 MHz		634		pF
Output Capacitance	C _{oss}			58		pF
Reverse Transfer Capacitance	C _{rss}			28		pF
Turn-On Delay Time	t _{d(on)}			7	14	ns
Turn-On Rise Time	t _r	V _{DD} = 40 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω (Note 2)		3	6	ns
Turn-Off Delay Time	t _{d(off)}			24	38	ns
Turn-Off Fall Time	t _f			4	8	ns
Total Gate Charge	Q _g	V _{DS} = 40 V, I _D = 4.0 A, V _{GS} = 10 V (Note 2)		13	18	nC
Gate-Source Charge	Q _{gs}			2.4		nC
Gate-Drain Charge	Q _{gd}			2.8		nC
Maximum Continuous Drain-Source Diode Forward Current	I _S				2.1	A
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _S = 2.1 A (Not 2)		0.8	1.2	V

Notes:

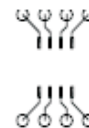
1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a) 50 °C/W when mounted on a 1in² pad of 2 oz copper



b) 105 °C/W when mounted on a 0.04 in² pad of 2 oz copper



c) 125 °C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%